FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-10191-2E

MEMORY

CMOS

256 K × 16 BITS HYPER PAGE MODE DYNAMIC RAM

MB81V4265S-60/-70/-60L/-70L

CMOS 262,144 × 16 BITS Hyper Page Mode Dynamic RAM

PRELIMINARY

■ DESCRIPTION

The Fujitsu MB81V4265S is a fully decoded CMOS Dynamic RAM (DRAM) that contains 4,194,304 memory cells accessible in 16-bit increments. The MB81V4265S features the “hyper page” mode of operation which provides extended valid time for data output and higher speed random access of up to 512 × 16-bits of data within the same row than the fast page mode. The MB81V4265S-60/-70/-60L/-70L DRAMs are ideally suited for memory applications such as embedded control, buffer, portable computers, and video imaging equipment where very low power dissipation and high bandwidth are basic requirements of the design.

The MB81V4265S is fabricated using silicon gate CMOS and Fujitsu's advanced four-layer polysilicon process. This process, coupled with three-dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes.

■ PRODUCT LINE & FEATURES

Parameter			MB81V4265S			
			-60	-60L	-70	-70L
$\overline{RAS}$ Access Time			60 ns max.		70 ns max.	
$\overline{CAS}$ Access Time			20 ns max.		20 ns max.	
Address Access Time			30 ns max.		35 ns max.	
Random Cycle Time			104 ns min.		119 ns min.	
Hyper Page Mode Cycle Time			25 ns min.		30 ns min.	
Low Power Dissipation	Operating Current		378 mW max.		335 mW max.	
	Standby Current	LVTTL Level	7.2 mW	3.6 mW	7.2 mW	3.6 mW
		CMOS Level	3.6 mW	540 µW	3.6 mW	540 µW

- 262,144 words × 16 bits organization
- Silicon gate, CMOS, Advanced Stacked Capacitor Cell
- All input and output are LVTTL compatible
- 512 refresh cycles every 8.2 ms
- 9 rows × 9 columns, addressing scheme
- Self refresh function
- Standard and low power versions
- Early Write or $\overline{OE}$ controlled Write capability
- $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Hyper page mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

MB81V4265S-60/-70/-60L/-70L

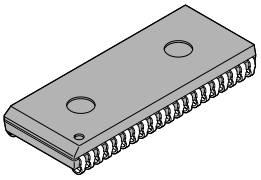
■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value	Unit
Voltage at Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	–0.5 to +4.6	V
Voltage of V_{CC} Supply Relative to V_{SS}	V_{CC}	–0.5 to +4.6	V
Power Dissipation	P_D	1.0	W
Short Circuit Output Current	I_{OUT}	–50 to +50	mA
Storage Temperature	T_{STG}	–55 to +125	°C
Temperature under Bias	T_{BIAS}	0 to +70	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

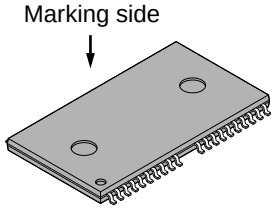
■ PACKAGE

Plastic SOJ Package



(LCC-40P-M01)

Plastic TSOP (II) Package

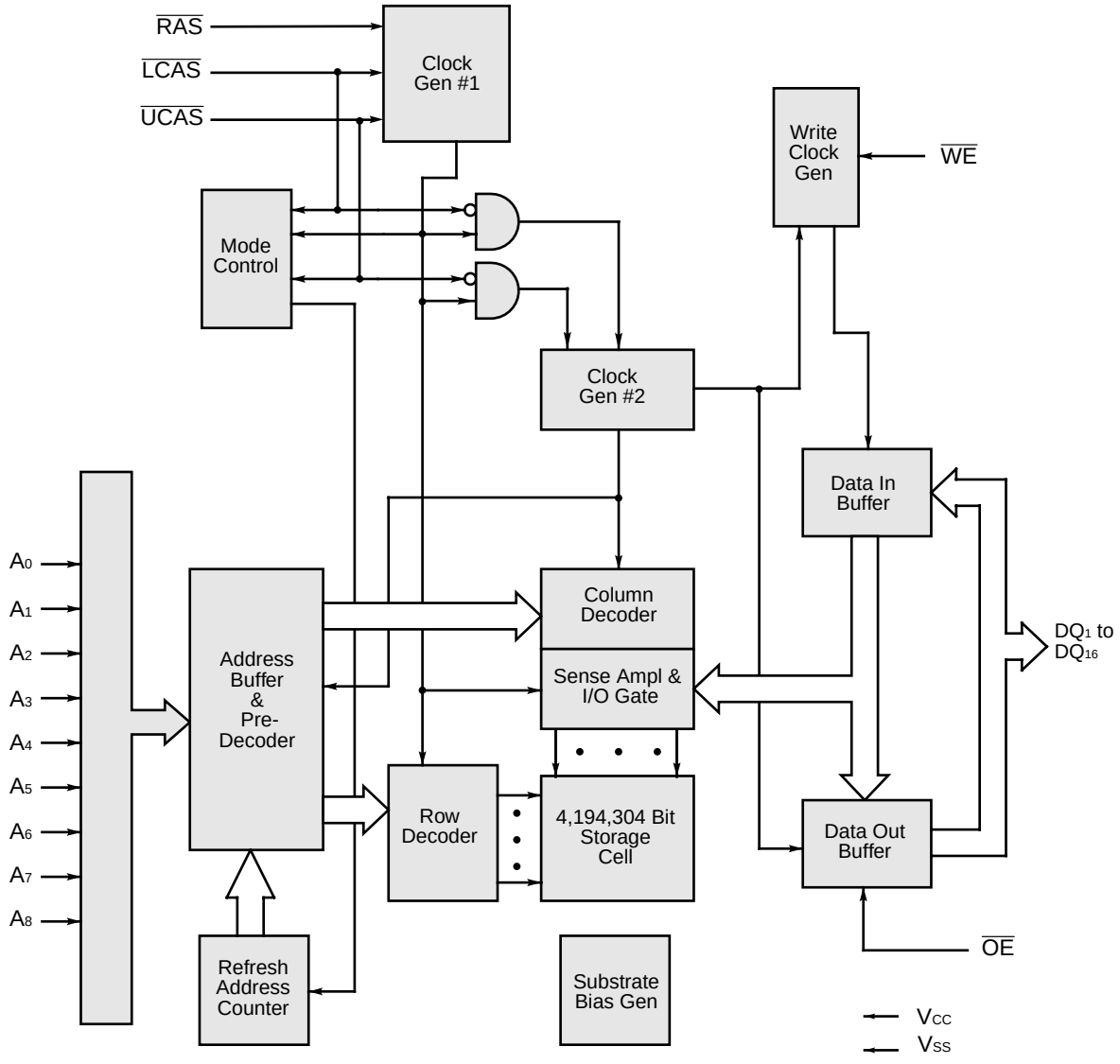


(FPT-44P-M07)
(Normal Bend)

Package and Ordering Information

– 40-pin plastic (400 mil) SOJ, order as MB81V4265S-××PJ and MB81V4265S-××LPJ (Low Power)
– 44-pin plastic (400 mil) TSOP (II) with normal bend leads, order as MB81V4265S-××PFTN and MB81V4265S-××LPFTN (Low Power)

Fig. 1 – MB81V4265S DYNAMIC RAM - BLOCK DIAGRAM



■ CAPACITANCE

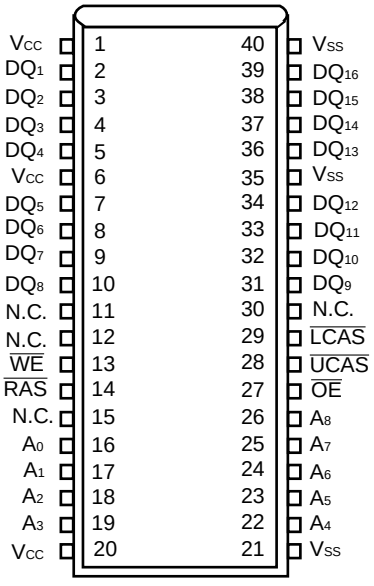
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance, A_0 to A_8	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$	C_{IN2}	—	5	pF
Input/Output Capacitance, DQ_1 to DQ_{16}	C_{DQ}	—	7	pF

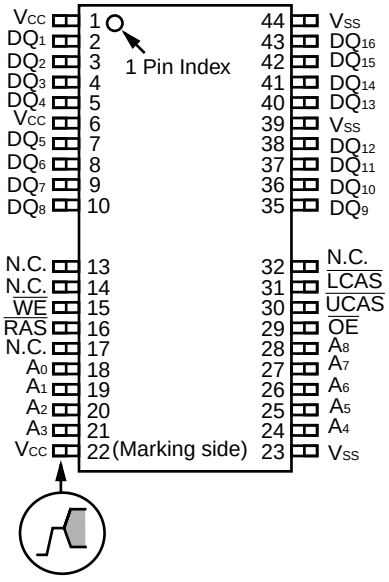
MB81V4265S-60/-70/-60L/-70L

■ PIN ASSIGNMENTS AND DESCRIPTIONS

40-Pin SOJ
(TOP VIEW)
<LCC-40P-M01>



44-Pin TSOP (II)
(TOP VIEW)
<Normal Bend: FPT-44P-M07>



Designator	Function
A_0 to A_8	Address inputs row : A_0 to A_8 column : A_0 to A_8 refresh : A_0 to A_8
$\overline{RAS}$	Row address strobe
$\overline{LCAS}$	Lower column address strobe
$\overline{UCAS}$	Upper column address strobe
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
DQ_1 to DQ_{16}	Data Input/ Output
V_{CC}	+3.3 volt power supply
V_{SS}	Circuit ground
N.C.	No connection

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min.	Typ.	Max.	Unit	Ambient Operating Temp.
Supply Voltage	*1	V_{CC}	3.0	3.3	3.6	V	0°C to +70°C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	*1	V_{IH}	–2.0	—	V_{CC}+0.3	V	
Input Low Voltage, all inputs*	*1	V_{IL}	–0.3	—	0.8	V	

* : Undershoots of up to –2.0 volts with a pulse width not exceeding 20 ns are acceptable.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

■ FUNCTIONAL OPERATION

ADDRESS INPUTS

Eighteen input bits are required to decode any sixteen of 4,194,304 cell addresses in the memory matrix. Since only nine address bits (A_0 to A_8) are available, the column and row inputs are separately strobed by $\overline{LCAS}$ or $\overline{UCAS}$ and $\overline{RAS}$ as shown in Figure 1. First, nine row address bits are input on pins A_0-through-A_8 and latched with the row address strobe ($\overline{RAS}$) then, nine column address bits are input and latched with the column address strobe ($\overline{LCAS}$ or $\overline{UCAS}$). Both row and column addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{LCAS}$ or $\overline{UCAS}$, respectively. The address latches are of the flow-through type; thus, address information appearing after t_{RAH} (min) + t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

Input data is written into memory in either of three basic ways : an early write cycle, an $\overline{OE}$ (delayed) write cycle, and a read-modify-write cycle. The falling edge of $\overline{WE}$ or $\overline{LCAS}$ / $\overline{UCAS}$, whichever is later, serves as the input data-latch strobe. In an early write cycle, the input data of DQ_1 to DQ_8 is strobed by $\overline{LCAS}$ and DQ_9 to DQ_{16} is strobed by $\overline{UCAS}$ and the setup/hold times are referenced to each $\overline{LCAS}$ and $\overline{UCAS}$ because $\overline{WE}$ goes Low before $\overline{LCAS}$ / $\overline{UCAS}$. In a delayed write or a read-modify-write cycle, $\overline{WE}$ goes Low after $\overline{LCAS}$ / $\overline{UCAS}$; thus, input data is strobed by $\overline{WE}$ and all setup/hold times are referenced to the write-enable signal.

DATA OUTPUT

The three-state buffers are LVTTL compatible with a fanout of one TTL load. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes Low. When a read or read-modify-write cycle is executed, valid outputs and High-Z state are obtained under the following conditions:

- t_{RAC} : from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.
- t_{CAC} : from the falling edge of $\overline{LCAS}$ (for DQ_1 to DQ_8) $\overline{UCAS}$ (for DQ_9 to DQ_{16}) when t_{RCD} is greater than t_{RCD} (max).
- t_{AA} : from column address input when t_{RAD} is greater than t_{RAD} (max), and t_{RCD} (max) is satisfied.
- t_{OEA} : from the falling edge of $\overline{OE}$ when $\overline{OE}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA}.
- t_{OEZ} : from $\overline{OE}$ inactive.
- t_{OFF} : from $\overline{CAS}$ inactive while $\overline{RAS}$ inactive.
- t_{OFR} : from $\overline{RAS}$ inactive while $\overline{CAS}$ inactive.
- t_{WEZ} : from $\overline{WE}$ active while $\overline{CAS}$ inactive.

The data goes a high-impedance state after either $\overline{OE}$ is inactive, or both $\overline{RAS}$ and $\overline{LCAS}$ (and/or $\overline{UCAS}$) are inactive, or $\overline{CAS}$ is reactived. When an early write is executed, the output buffers remain in a high-impedance state during the entire cycle.

HYPER PAGE MODE OPERATION

The hyper page mode operation provides faster memory access and lower power dissipation. The hyper page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions, $\overline{RAS}$ is held Low for all contiguous memory cycles in which row addresses are common. For each page of memory (within column address locations), any of 512 $\times$ 16-bits can be accessed and, when multiple MB81V4265Ss are used, $\overline{CAS}$ is decoded to select the desired memory page. Hyper page mode operations need not be addressed sequentially and combinations of read, write, and/or read-modify-write cycles are permitted. Hyper page mode features that output remains valid when $\overline{CAS}$ is inactive until $\overline{CAS}$ is reactivated.

■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Note 3

Parameter	Notes		Symbol	Condition	Value			Unit
					Min.	Max.		
						Std Power	Low Power	
Output High Voltage	*1		V_{OH}	I_{OH} = –2.0 mA	2.4	—	—	V
Output Low Voltage	*1		V_{OL}	I_{OL} = 2.0 mA	—	0.4	0.4	
Input Leakage Current (Any Input)			$I_{I(L)}$	0 V ≤ V_{IN} ≤ 3.6 V; 3.0 V ≤ V_{CC} ≤ 3.6 V; V_{SS} = 0 V; All other pins not under test = 0 V	–10	10	10	µA
Output Leakage Current			$I_{DQ(L)}$	0 V ≤ V_{OUT} ≤ 3.6 V; Data out disabled	–10	10	10	
Operating Current (Average Power Supply Current)	*2	MB81V4265S-60/60L	I_{CC1}	$\overline{RAS}$, $\overline{LCAS}$ & $\overline{UCAS}$ cycling; t_{RC} = min	—	105	105	mA
		MB81V4265S-70/70L				93	93	
Standby Current (Power Supply Current)		LVTTL Level	I_{CC2}	$\overline{RAS}$ = $\overline{LCAS}$ = $\overline{UCAS}$ = V_{IH}	—	2.0	1.0	mA
		CMOS Level		$\overline{RAS}$ = $\overline{LCAS}$ = $\overline{UCAS}$ ≥ V_{CC} –0.2 V		1000	150	µA
Refresh Current #1 (Average Power Supply Current)	*2	MB81V4265S-60/60L	I_{CC3}	$\overline{LCAS}$ = $\overline{UCAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min	—	105	105	mA
		MB81V4265S-70/70L				93	93	
Hyper Page Mode Current	*2	MB81V4265S-60/60L	I_{CC4}	$\overline{RAS}$ = V_{IL}, $\overline{LCAS}$ / $\overline{UCAS}$ cycling; t_{HPC} = min	—	105	105	mA
		MB81V4265S-70/70L				93	93	
Refresh Current #2 (Average Power Supply Current)	*2	MB81V4265S-60/60L	I_{CC5}	$\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	—	105	105	mA
		MB81V4265S-70/70L				93	93	
Refresh Current #3 (Average Power Supply Current)		MB81V4265S-60/60L	I_{CC6}	$\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = 125 µs, t_{RAS} = min to 1 µs, V_{IH} ≥ V_{CC} – 0.2 V	—	—	250	µA
		MB81V4265S-70/70L			—	—	250	
Refresh Current #4 (Average Power Supply Current)		MB81V4265S-60/60L	I_{CC9}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = V_{IL} Self refresh; t_{RASS} = min	—	1000	250	µA
		MB81V4265S-70/70L						

MB81V4265S-60/-70/-60L/-70L

■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81V4265S-60/60L		MB81V4265S-70/70L		Unit
				Min.	Max.	Min.	Max.	
1	Time Between Refresh	Std Power	t_{REF}	—	8.2	—	8.2	ms
		Low Power		—	64	—	64	
2	Random Read/Write Cycle Time		t_{RC}	104	—	119	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	138	—	158	—	ns
4	Access Time from $\overline{RAS}$	*6,9	t_{RAC}	—	60	—	70	ns
5	Access Time from $\overline{CAS}$	*7,9	t_{CAC}	—	20	—	20	ns
6	Column Address Access Time	*8,9	t_{AA}	—	30	—	35	ns
7	Output Hold Time		t_{OH}	5	—	5	—	ns
8	Output Hold Time from $\overline{CAS}$		t_{OHC}	5	—	5	—	ns
9	Output Buffer Turn On Delay Time		t_{ON}	0	—	0	—	ns
10	Output Buffer Turn Off Delay Time	*10	t_{OFF}	—	15	—	15	ns
11	Output Buffer Turn Off Delay Time from $\overline{RAS}$		t_{OFR}	—	15	—	15	ns
12	Output Buffer Turn Off Delay Time from $\overline{WE}$		t_{WEZ}	—	15	—	15	ns
13	Transition Time		t_T	1	50	1	50	ns
14	$\overline{RAS}$ Precharge Time		t_{RP}	40	—	45	—	ns
15	$\overline{RAS}$ Pulse Width		t_{RAS}	60	100000	70	100000	ns
16	$\overline{RAS}$ Hold Time		t_{RSH}	20	—	20	—	ns
17	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	*21	t_{CRP}	0	—	0	—	ns
18	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	*11,12, 22	t_{RCD}	14	40	14	50	ns
19	$\overline{CAS}$ Pulse Width		t_{CAS}	10	—	10	—	ns
20	$\overline{CAS}$ Hold Time		t_{CSH}	40	—	50	—	ns
21	$\overline{CAS}$ Precharge Time (Normal)	*19	t_{CPN}	10	—	10	—	ns
22	Row Address Set Up Time		t_{ASR}	0	—	0	—	ns
23	Row Address Hold Time		t_{RAH}	10	—	10	—	ns
24	Column Address Set Up Time		t_{ASC}	0	—	0	—	ns
25	Column Address Hold Time		t_{CAH}	10	—	10	—	ns
26	$\overline{RAS}$ to Column Address Delay Time	*13	t_{RAD}	12	30	12	35	ns
27	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	30	—	35	—	ns
28	Column Address to $\overline{CAS}$ Lead Time		t_{CAL}	23	—	28	—	ns
29	Read Command and Set Up Time		t_{RCS}	0	—	0	—	ns
30	Read Command Hold Time Referenced to $\overline{RAS}$	*14	t_{RRH}	0	—	0	—	ns

(Continued)

MB81V4265S-60/-70/-60L/-70L

No.	Parameter	Notes	Symbol	MB81V4265S-60/60L		MB81V4265S-70/70L		Unit
				Min.	Max.	Min.	Max.	
31	Read Command Hold Time Referenced to $\overline{CAS}$	*14	t_{RCH}	0	—	0	—	ns
32	Write Command Set Up Time	*15	t_{WCS}	0	—	0	—	ns
33	Write Command Hold Time		t_{WCH}	10	—	10	—	ns
34	$\overline{WE}$ Pulse Width		t_{WP}	10	—	10	—	ns
35	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	15	—	20	—	ns
36	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	10	—	10	—	ns
37	DIN Set Up Time		t_{DS}	0	—	0	—	ns
38	DIN Hold Time		t_{DH}	10	—	10	—	ns
39	$\overline{RAS}$ to $\overline{WE}$ Delay Time		t_{RWD}	77	—	87	—	ns
40	$\overline{CAS}$ to $\overline{WE}$ Delay Time		t_{CWD}	37	—	37	—	ns
41	Column Address to $\overline{WE}$ Delay Time		t_{AWD}	47	—	52	—	ns
42	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)		t_{RPC}	10	—	10	—	ns
43	$\overline{CAS}$ Set Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	ns
44	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CHR}	10	—	10	—	ns
45	Access Time from $\overline{OE}$	*9	t_{OEA}	—	20	—	20	ns
46	Output Buffer Turn Off Delay from $\overline{OE}$	*10	t_{OEZ}	—	15	—	15	ns
47	$\overline{OE}$ to $\overline{RAS}$ Lead Time for Valid Data		t_{OEL}	10	—	10	—	ns
48	$\overline{OE}$ to $\overline{CAS}$ Lead Time		t_{COL}	5	—	5	—	ns
49	$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	*16	t_{OEH}	0	—	0	—	ns
50	$\overline{OE}$ to Data in Delay Time		t_{OED}	15	—	15	—	ns
51	DIN to $\overline{CAS}$ Delay Time	*17	t_{DZC}	0	—	0	—	ns
52	DIN to $\overline{OE}$ Delay Time	*17	t_{DZO}	0	—	0	—	ns
53	$\overline{CAS}$ to Data in Delay Time		t_{CDD}	15	—	15	—	ns
54	$\overline{RAS}$ to Data in Delay Time		t_{RDD}	15	—	15	—	ns
55	Column Address Hold Time from $\overline{RAS}$		t_{AR}	26	—	26	—	ns
56	Write Command Hold Time from $\overline{RAS}$		t_{WCR}	24	—	24	—	ns
57	DIN Hold Time Referenced to $\overline{RAS}$		t_{DHR}	24	—	24	—	ns
58	$\overline{OE}$ Precharge Time		t_{OEP}	10	—	10	—	ns
59	$\overline{OE}$ Hold Time Referenced to $\overline{CAS}$		t_{OECH}	10	—	10	—	ns
60	$\overline{WE}$ Precharge Time		t_{WPZ}	10	—	10	—	ns

(Continued)

MB81V4265S-60/-70/-60L/-70L

(Continued)

No.	Parameter	Notes	Symbol	MB81V4265S-60/60L		MB81V4265S-70/70L		Unit
				Min.	Max.	Min.	Max.	
61	$\overline{WE}$ to Data in Delay Time		t_{WED}	15	—	15	—	ns
62	Hyper Page Mode $\overline{RAS}$ Pulse Width		t_{RASP}	60	200000	70	200000	ns
63	Hyper Page Mode Read/Write Cycle Time		t_{HPC}	25	—	30	—	ns
64	Hyper Page Mode Read-Modify-Write Cycle Time		t_{HPRWC}	66	—	71	—	ns
65	Access Time from $\overline{CAS}$ Precharge	*9,18	t_{CPA}	—	35	—	40	ns
66	Hyper Page Mode $\overline{CAS}$ Pulse Width		t_{CP}	10	—	10	—	ns
67	Hyper Page Mode $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge		t_{RHCP}	35	—	40	—	ns
68	Hyper Page Mode $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time		t_{CPWD}	52	—	57	—	ns

Notes: *1. Referenced to V_{SS}. To all V_{CC} (V_{SS}) pins, the same supply voltage should be applied.

*2. I_{CC} depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
I_{CC} depends on the number of address change as $\overline{RAS} = V_{IL}$ and $\overline{UCAS} = V_{IH}$, $\overline{LCAS} = V_{IH}$, $V_{IL} > -0.3$ V.
I_{CC1}, I_{CC3} and I_{CC5} are specified at one time of address change during $\overline{RAS} = V_{IL}$ and $\overline{UCAS} = V_{IH}$, $\overline{LCAS} = V_{IH}$.
I_{CC4} is specified at one time of address change during one Page cycle.

*3. An initial pause ($\overline{RAS} = \overline{CAS} = V_{IH}$) of 200 µs is required after power-up followed by any eight $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

*4. AC characteristics assume t_T = 2 ns.

*5. Input voltage levels are 0 V and 3.0 V, and input reference levels are V_{IH} (min) and V_{IL} (max) for measuring timing of input signals. Also, the transition time(t_T) is measured between V_{IH} (min) and V_{IL} (max).
The output reference levels are V_{OH} = 2.0 V and V_{OL} = 0.8 V.

*6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.

*7. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.

*8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.

*9. Measured with a load equivalent to one TTL load and 50 pF (60 ns version).
Measured with a load equivalent to one TTL and 100 pF (70 ns version).

*10. t_{OFF} and t_{OEZ} are specified that output buffer change to high-impedance state.

*11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

*12. t_{RCD} (min) = t_{RAH} (min) + 2 t_T + t_{ASC} (min).

*13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

*14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

*15. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.

*16. Assumes that $t_{WCS} < t_{WCS}$ (min).

*17. Either t_{DZC} or t_{DZO} must be satisfied.

*18. t_{CPA} is access time from the selection of a new column address (that is caused by changing both $\overline{UCAS}$ and $\overline{LCAS}$ from "L" to "H"). Therefore, if t_{CP} is long, t_{CPA} is longer than t_{CPA} (max).

*19. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh.

*20. The last $\overline{CAS}$ rising edge.

*21. The first $\overline{CAS}$ falling edge.

MB81V4265S-60/-70/-60L/-70L

Fig. 2 – t_{RAC} vs. t_{RCD}

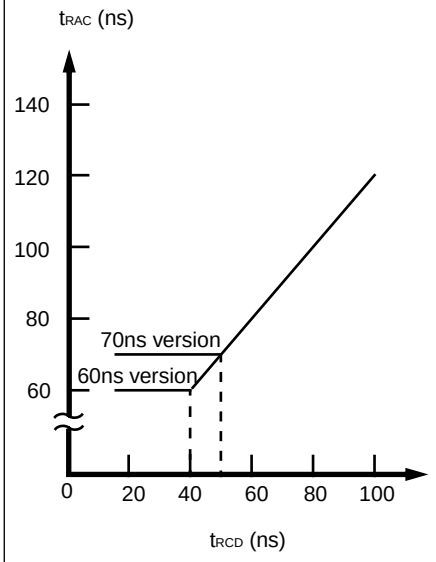


Fig. 3 – t_{RAC} vs. t_{RAD}

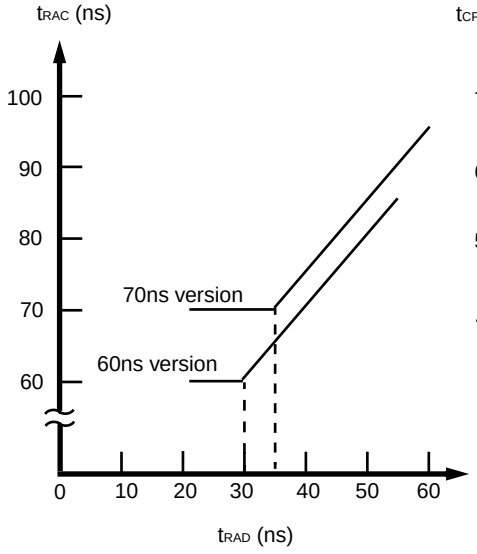
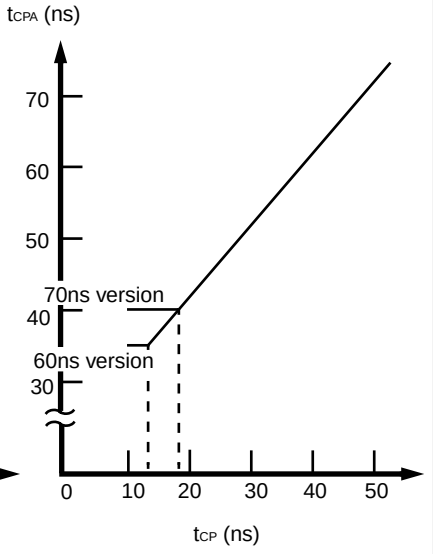


Fig. 4 – t_{CPA} vs. t_{CP}

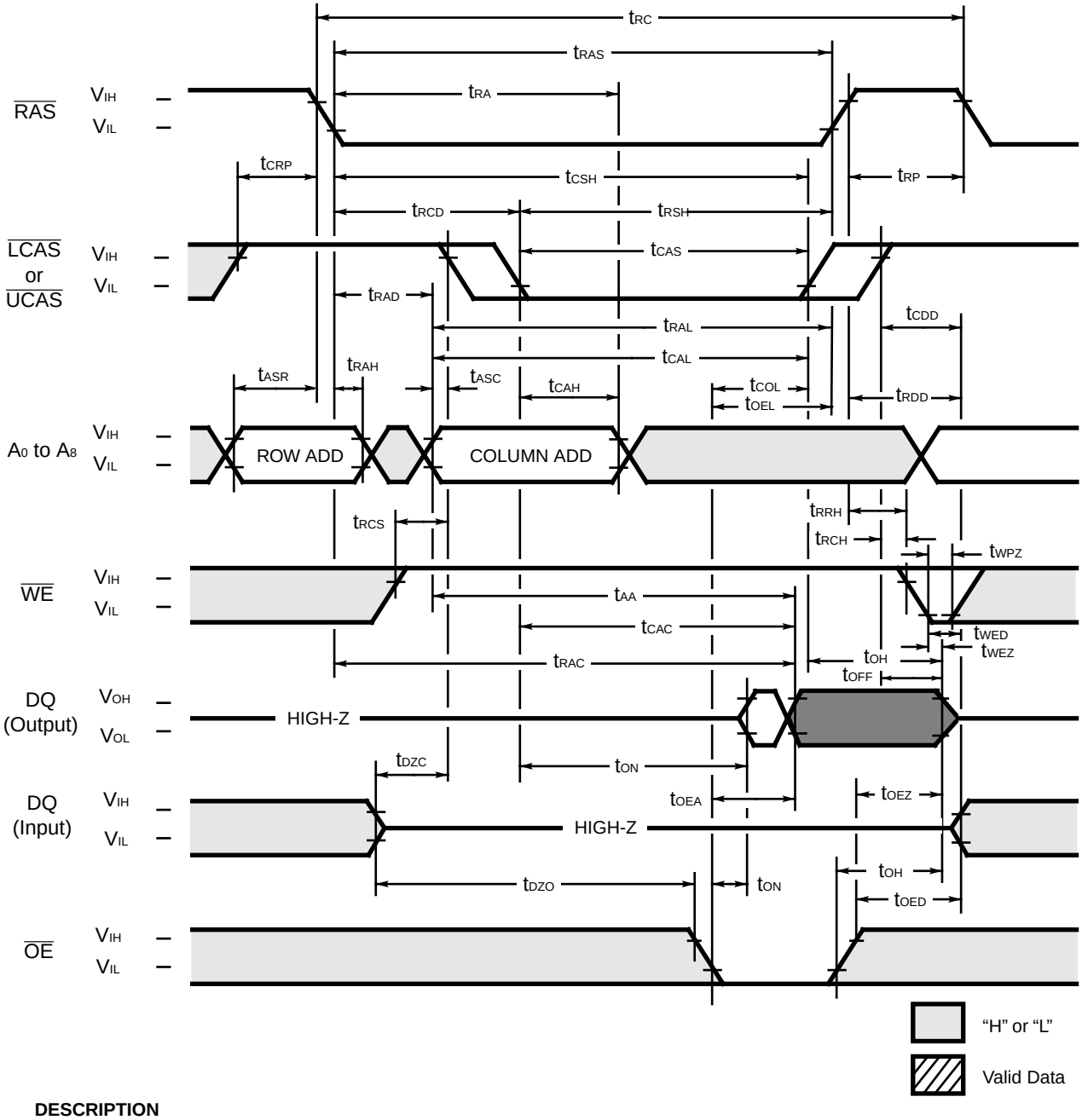


■ FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input					Address Input		Input/Output Data				Refresh	Note
								DQ_1 to DQ_8		DQ_9 to DQ_{16}			
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	Row	Column	Input	Output	Input	Output		
Standby	H	H	H	X	X	—	—	—	High-Z	—	High-Z	—	
Read Cycle	L	L H L	H L L	H	L	Valid	Valid	—	Valid High-Z Valid	—	High-Z Valid Valid	Yes*	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L H L	H L L	L	X	Valid	Valid	Valid — Valid	High-Z	— Valid Valid	High-Z	Yes*	$t_{WCS} \geq t_{WCS}$ (min)
Read-Modify-Write Cycle	L	L H L	H L L	H→L	L→H	Valid	Valid	Valid — Valid	Valid High-Z Valid	— Valid Valid	High-Z Valid Valid	Yes*	
$\overline{RAS}$-only Refresh Cycle	L	H	H	X	X	Valid	—	—	High-Z	—	High-Z	Yes	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	L	L	L	X	X	—	—	—	High-Z	—	High-Z	Yes	$t_{CSR} \geq t_{CSR}$(min)
Hidden Refresh Cycle	H→L	L H L	H L L	H	L	—	—	—	Valid High-Z Valid	—	High-Z Valid Valid	Yes	Previous data is kept.

X : "H" or "L"
* : It is impossible in Hyper Page Mode.

Fig. 5 – READ CYCLE



DESCRIPTION

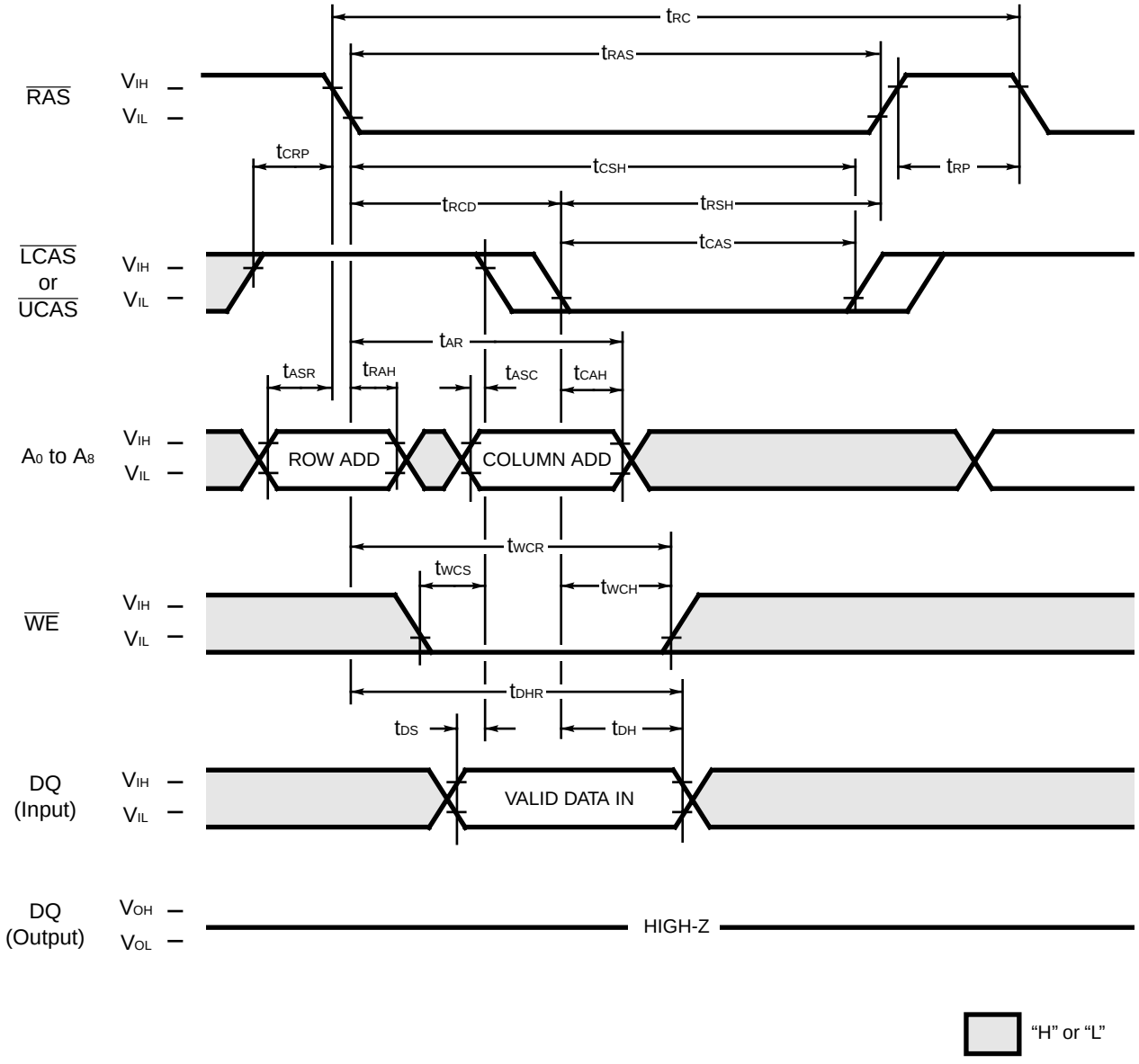
To implement a read operation, a valid address is latched by the $\overline{RAS}$ and $\overline{LCAS}$ or $\overline{UCAS}$ address strobes and with $\overline{WE}$ set to a High level and $\overline{OE}$ set to a low level, the output is valid once the memory access time has elapsed. DQ_8 to DQ_{16} pins is valid when $\overline{RAS}$ and $\overline{CAS}$ are High or until $\overline{OE}$ goes High. The access time is determined by $\overline{RAS}$(t_{RAC}), $\overline{LCAS}$/$\overline{UCAS}$(t_{CAC}), $\overline{OE}$(t_{OEA}) or column addresses (t_{AA}) under the following conditions:

If $t_{RCD} > t_{RCD}$ (max), access time = t_{CAC}.
If $t_{RAD} > t_{RAD}$ (max), access time = t_{AA}.
If $\overline{OE}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA} (whichever occurs later), access time = t_{OEA}.

However, if either $\overline{LCAS}$/$\overline{UCAS}$ or $\overline{OE}$ goes High, the output returns to a high-impedance state after t_{OH} is satisfied.

MB81V4265S-60/-70/-60L/-70L

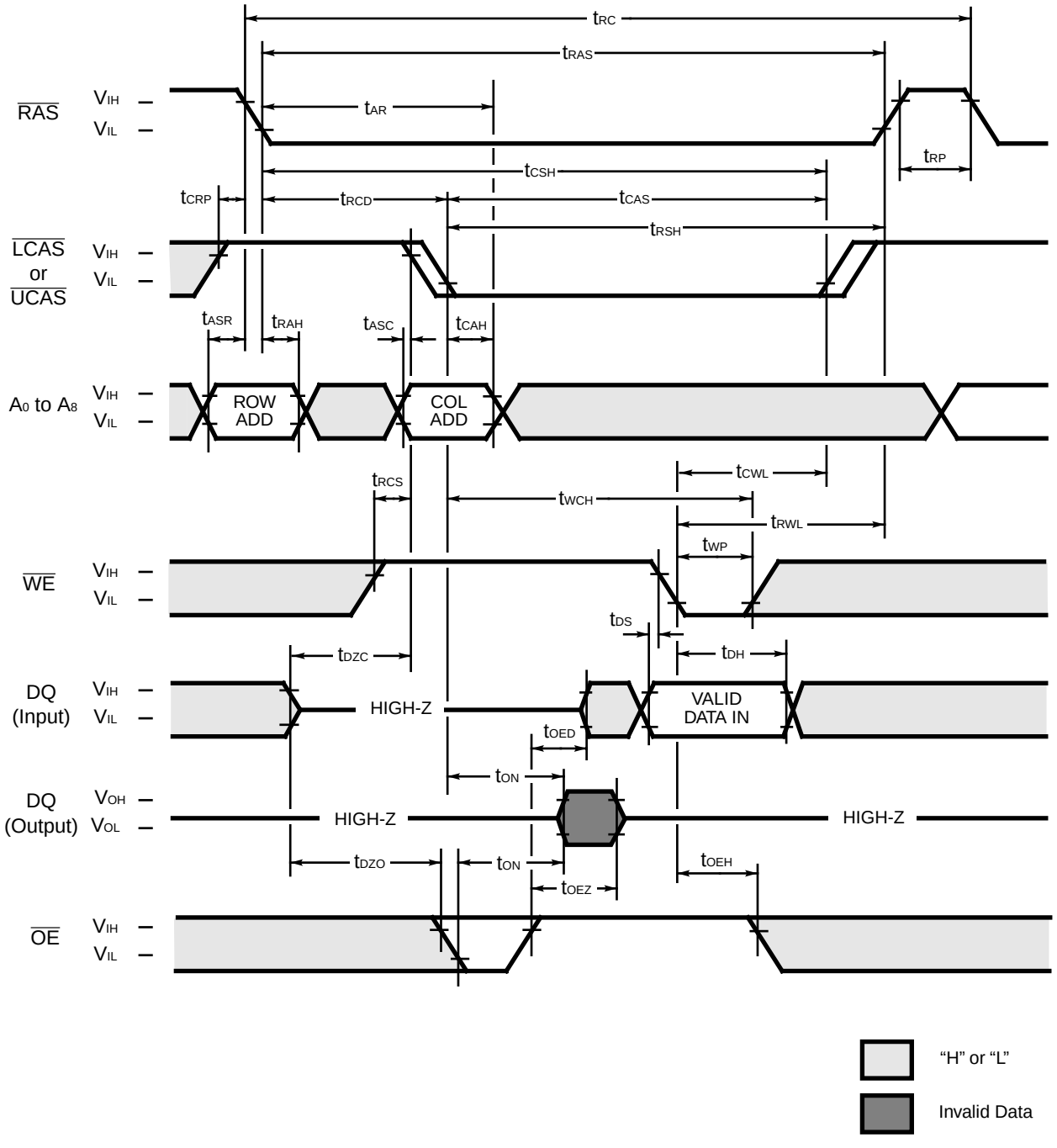
Fig. 6 – EARLY WRITE CYCLE



DESCRIPTION

A write cycle is similar to a read cycle except $\overline{WE}$ is set to a Low state and $\overline{OE}$ is an "H" or "L" signal. A write cycle can be implemented in either of three ways – early write, delayed write, or read-modify-write. During all write cycles, timing parameters t_{RWL}, t_{CWL}, t_{RAL} and t_{CAL} must be satisfied. In the early write cycle shown above t_{WCS} satisfied, data on the DQ pins are latched with the falling edge of $\overline{LCAS}$ or $\overline{UCAS}$ and written into memory.

Fig. 7 – DELAYED WRITE CYCLE ($\overline{OE}$ CONTROLLED)

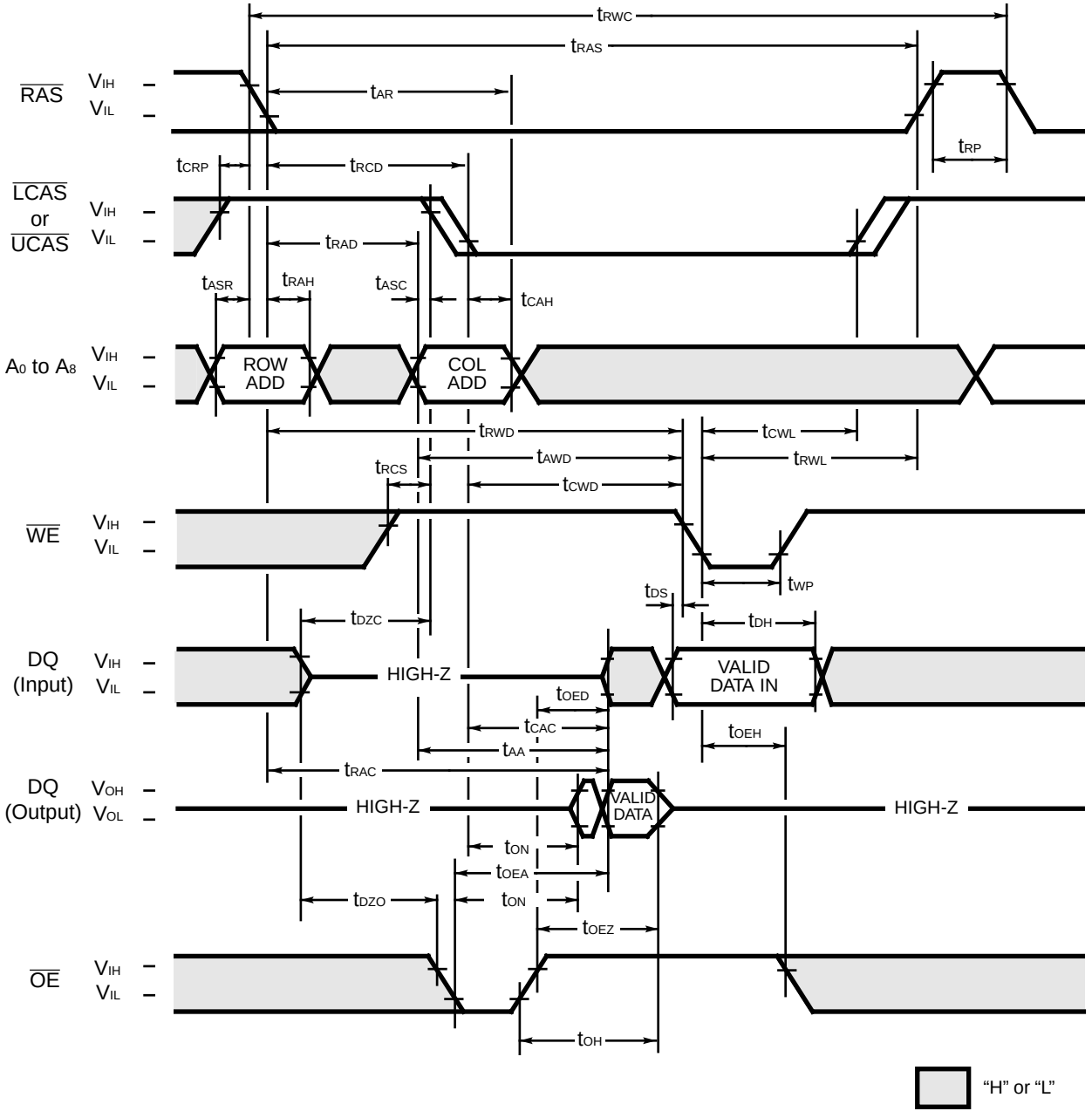


DESCRIPTION

In the delayed write cycle, t_{WCS} is not satisfied; thus, the data on the DQ pins are latched with the falling edge of $\overline{WE}$ and written into memory. The Output Enable ($\overline{OE}$) signal must be changed from Low to High before $\overline{WE}$ goes Low ($t_{OED} + t_T + t_{DS}$).

MB81V4265S-60/-70/-60L/-70L

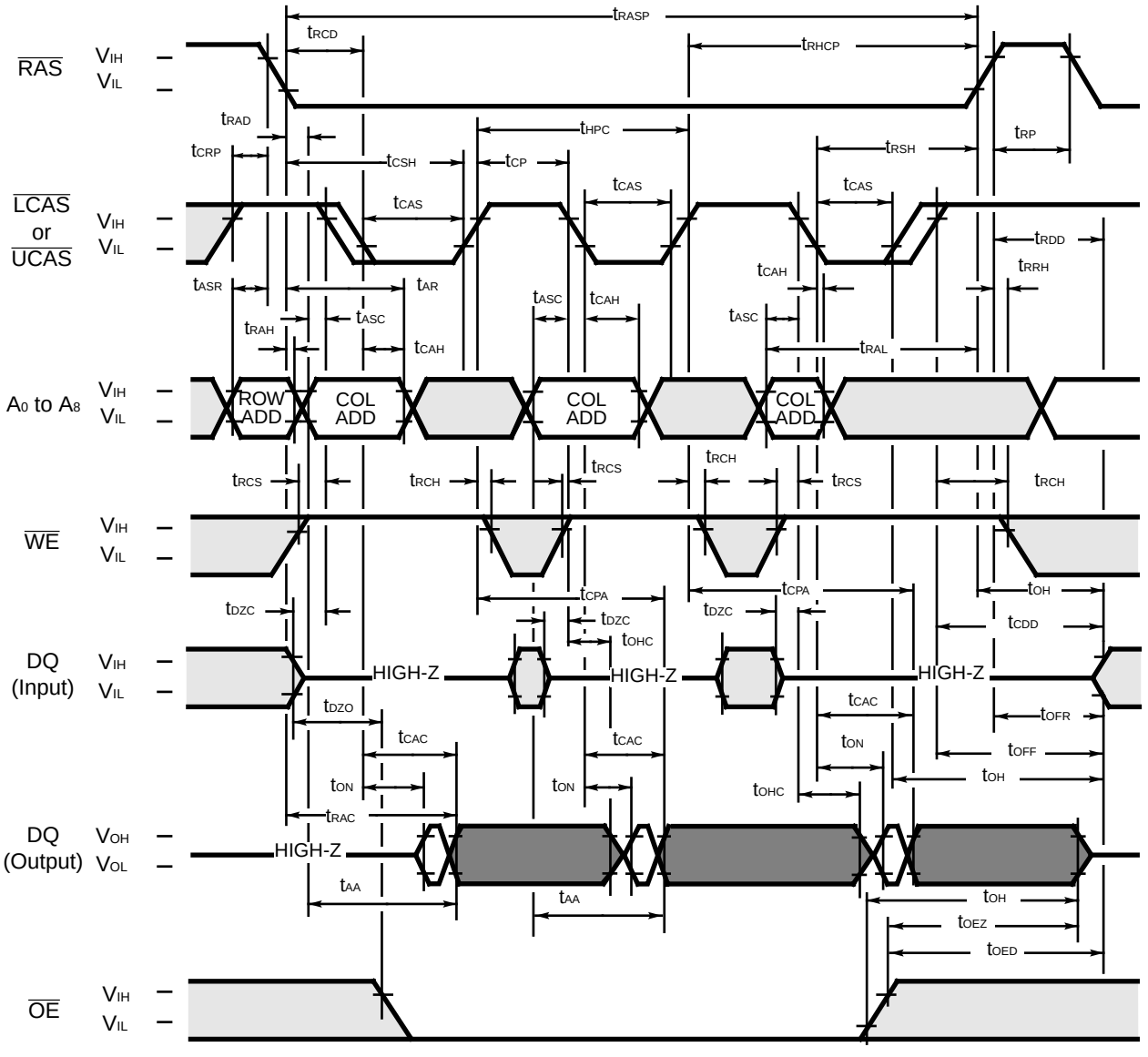
Fig. 8 – READ-MODIFY-WRITE CYCLE



DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from High to Low after the data appears on the DQ pins. In the read-modify-write cycle, $\overline{OE}$ must be changed from Low to High after the memory access time.

Fig. 9 – HYPER PAGE MODE READ CYCLE



During one cycle is achieved, the input/output timing apply the same manner as the former cycle.

"H" or "L"

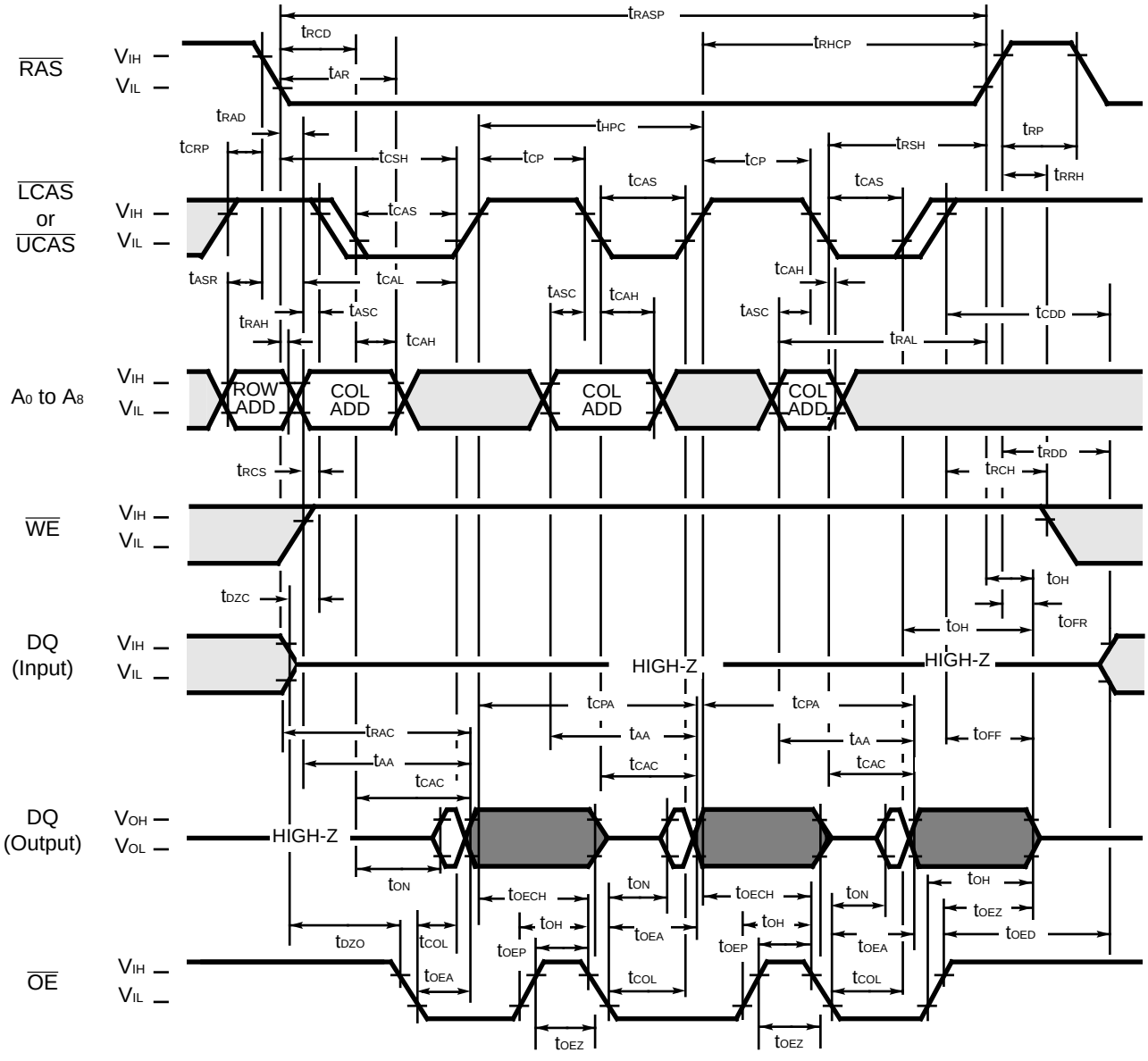
Valid Data

DESCRIPTION

The hyper page mode of operation permits faster successive memory operations at multiple column locations of the same row address.
This operation is performed by strobing in the row address and maintaining $\overline{RAS}$ at a Low level and $\overline{WE}$ at a High level during all successive memory cycles in which the row address is latched. The access time is determined by t_{CAC}, t_{AA}, t_{CPA}, or t_{OEA}, whichever one is the latest in occurring.

MB81V4265S-60/-70/-60L/-70L

Fig. 10 – HYPER PAGE MODE READ CYCLE ($\overline{OE}$ = "H" or "L")



During one cycle is achieved, the input/output timing apply the same manner as the former cycle.

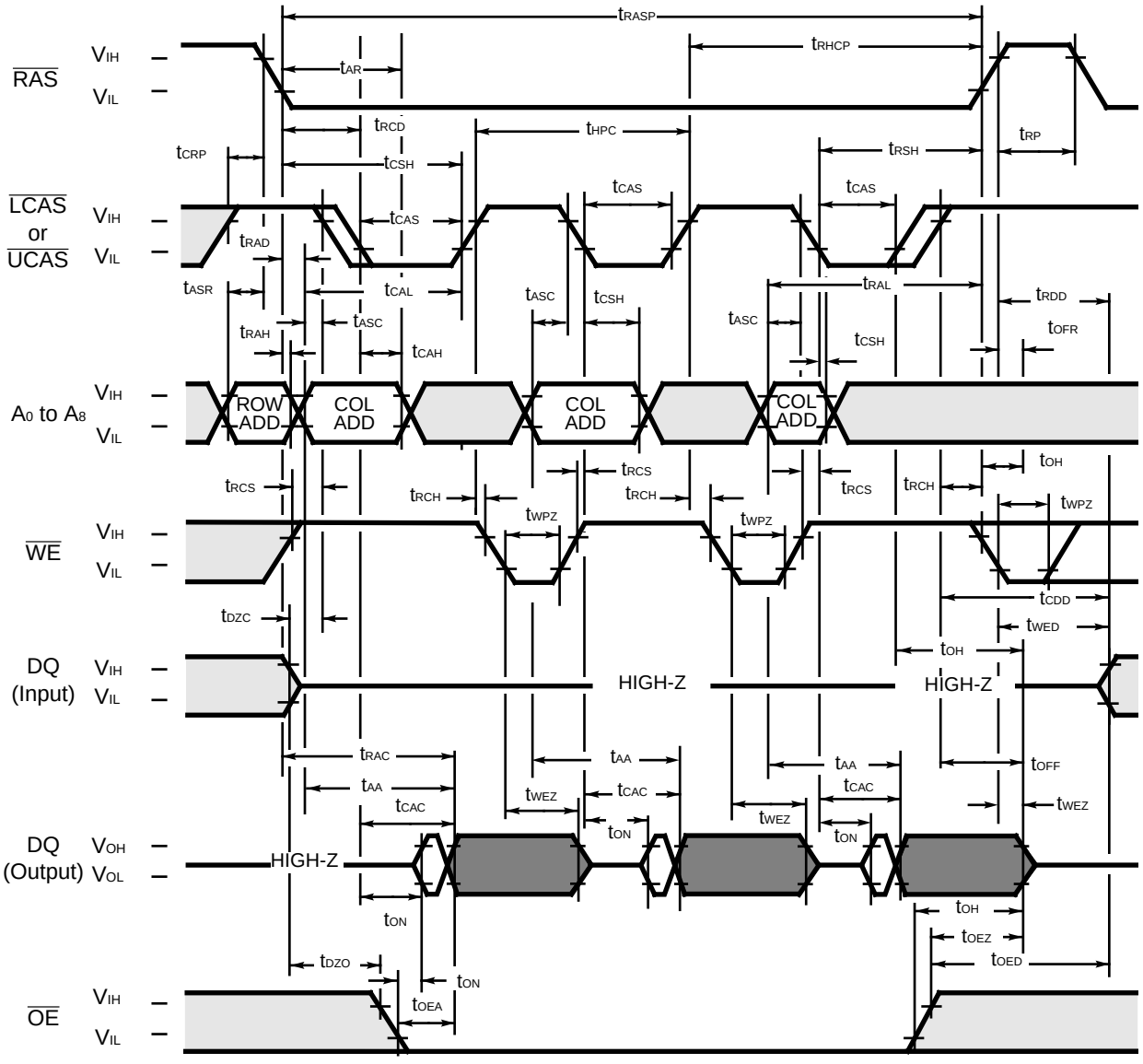
"H" or "L"

Valid Data

DESCRIPTION

The hyper page mode of operation permits faster successive memory operations at multiple column locations of the same row address.
This operation is performed by strobing in the row address and maintaining $\overline{RAS}$ at a Low level and $\overline{WE}$ at a High level during all successive memory cycles in which the row address is latched. The access time is determined by t_{CAC}, t_{AA}, t_{CPA}, or t_{OEA}, whichever one is the latest in occurring.

Fig. 11 – HYPER PAGE MODE READ CYCLE ($\overline{WE}$ = "H" or "L")



During one cycle is achieved, the input/output timing apply the same manner as the former cycle.

"H" or "L"

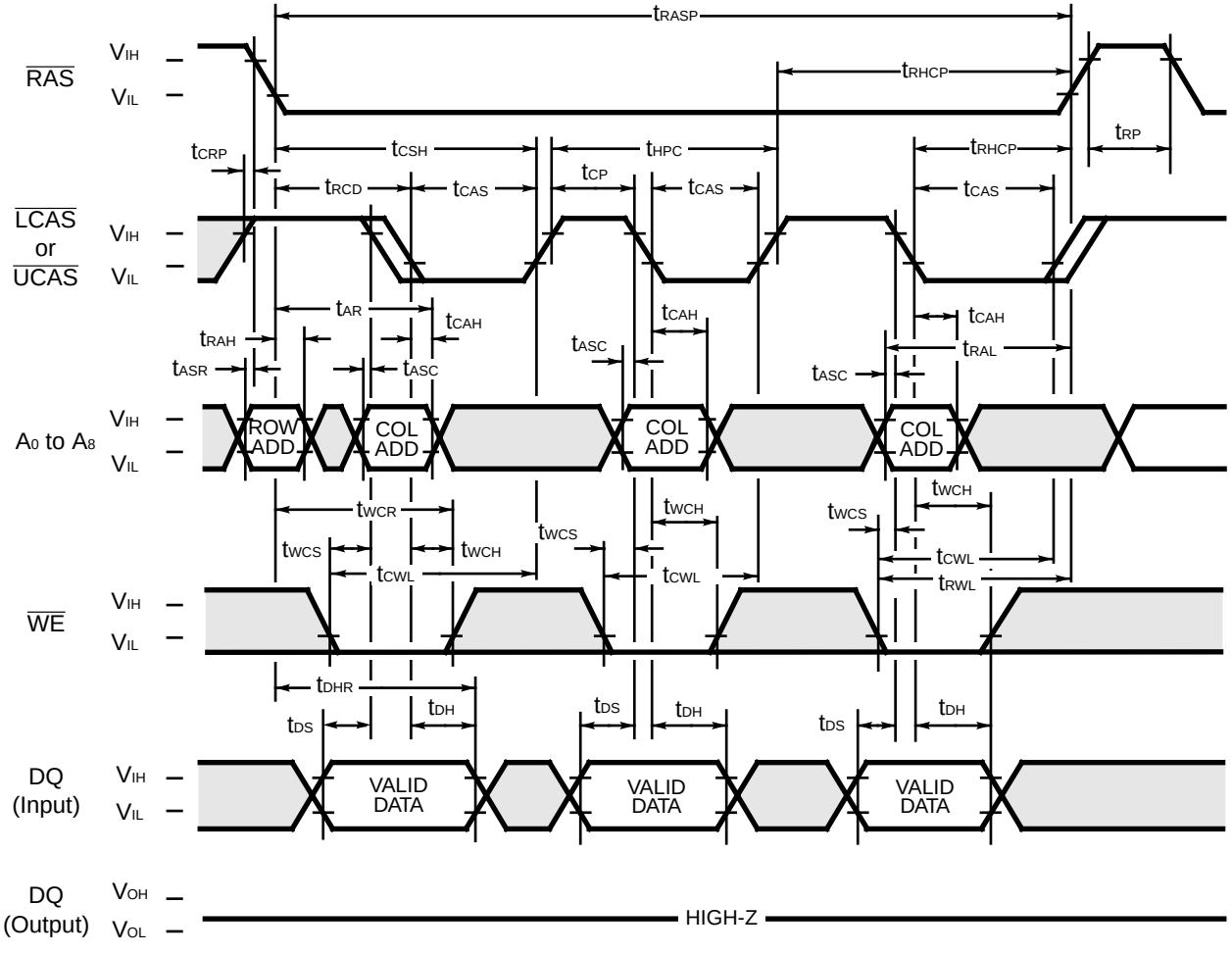
Valid Data

DESCRIPTION

The hyper page mode of operation permits faster successive memory operations at multiple column locations of the same row address.
This operation is performed by strobing in the row address and maintaining $\overline{RAS}$ at a Low level and $\overline{WE}$ at a High level during all successive memory cycles in which the row address is latched. The access time is determined by t_{CAC}, t_{AA}, t_{CPA}, or t_{OEA}, whichever one is the latest in occurring.

MB81V4265S-60/-70/-60L/-70L

Fig. 12 – HYPER PAGE MODE EARLY WRITE CYCLE



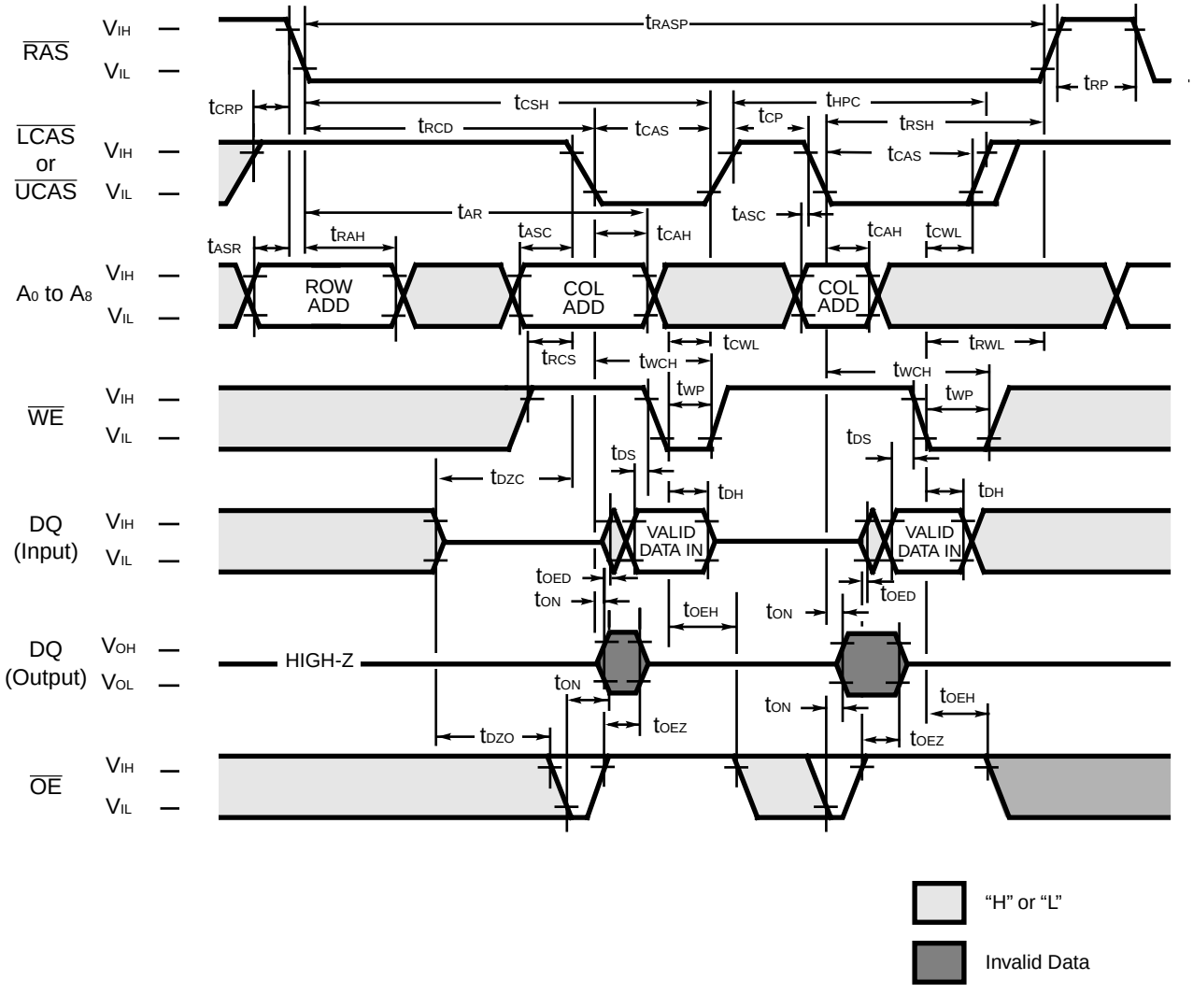
During one cycle is achieved, the input/output timing apply the same manner as the former cycle.

"H" or "L"

DESCRIPTION

The hyper page mode early write cycle is executed in the same manner as the hyper page mode read cycle except the states of $\overline{WE}$ and $\overline{OE}$ are reversed. Data appearing on the DQ_1 to DQ_8 is latched on the falling edge of $\overline{LCAS}$ and one appearing on the DQ_9 to DQ_{16} is latched on the falling edge of $\overline{UCAS}$ and the data is written into the memory. During the hyper page mode early write cycle, including the delayed ($\overline{OE}$) write and read-modify-write cycles, t_{CWL} must be satisfied.

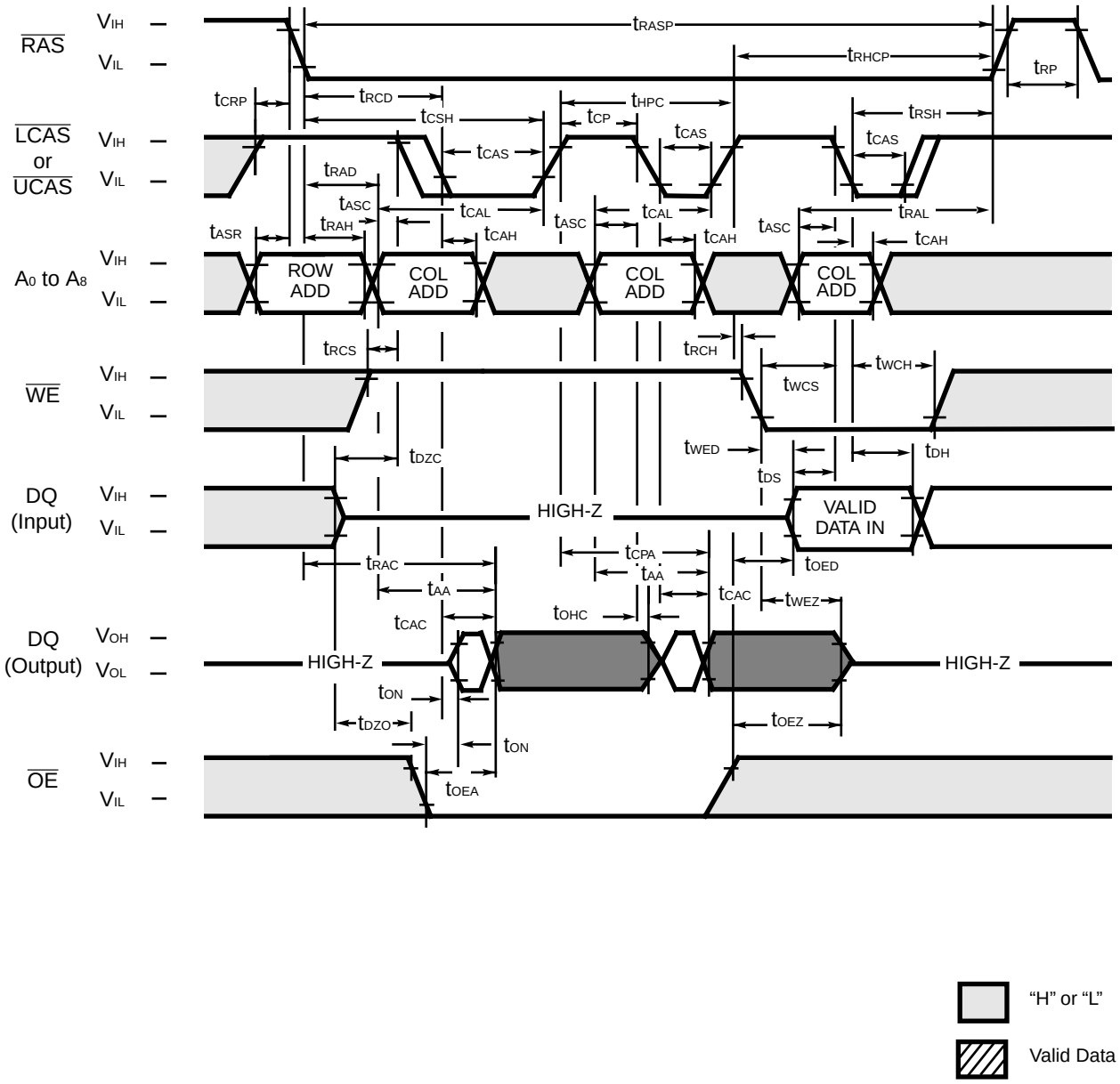
Fig. 13 – HYPER PAGE MODE DELAYED WRITE CYCLE



DESCRIPTION

The hyper page mode delayed write cycle is executed in the same manner as the hyper page mode early write cycle except for the states of $\overline{WE}$ and $\overline{OE}$. Input data on the DQ pins are latched on the falling edge of $\overline{WE}$ and written into memory. In the hyper page mode delayed write cycle, $\overline{OE}$ must be changed from Low to High before $\overline{WE}$ goes Low ($t_{OED} + t_T + t_{DS}$).

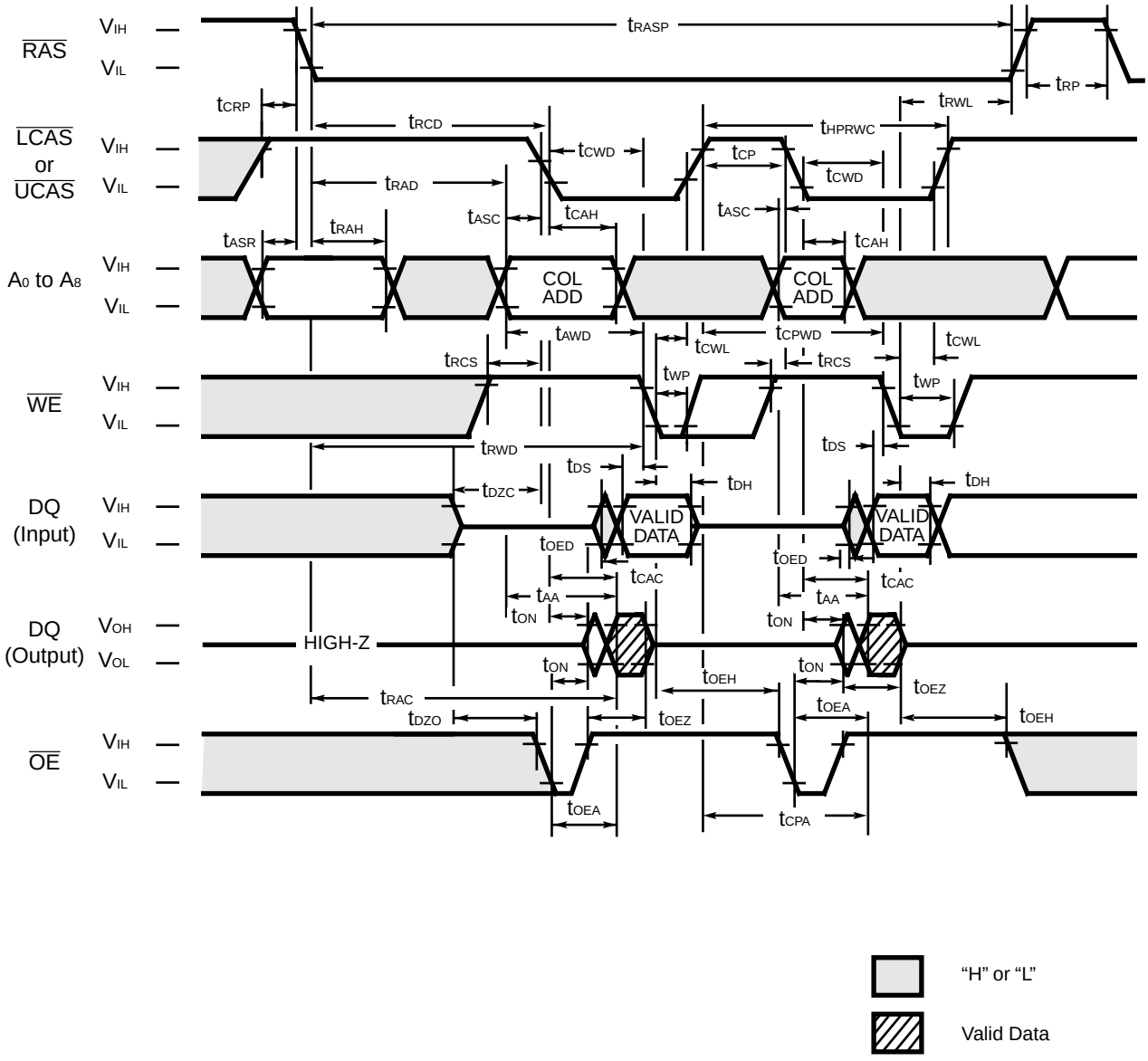
Fig. 14 – HYPER PAGE MODE READ/WRITE MIXED CYCLE



DESCRIPTION

The hyper page mode performs read/write operations repetitively during one $\overline{RAS}$ cycle. At this time, t_{HPC} (min) is invalid.

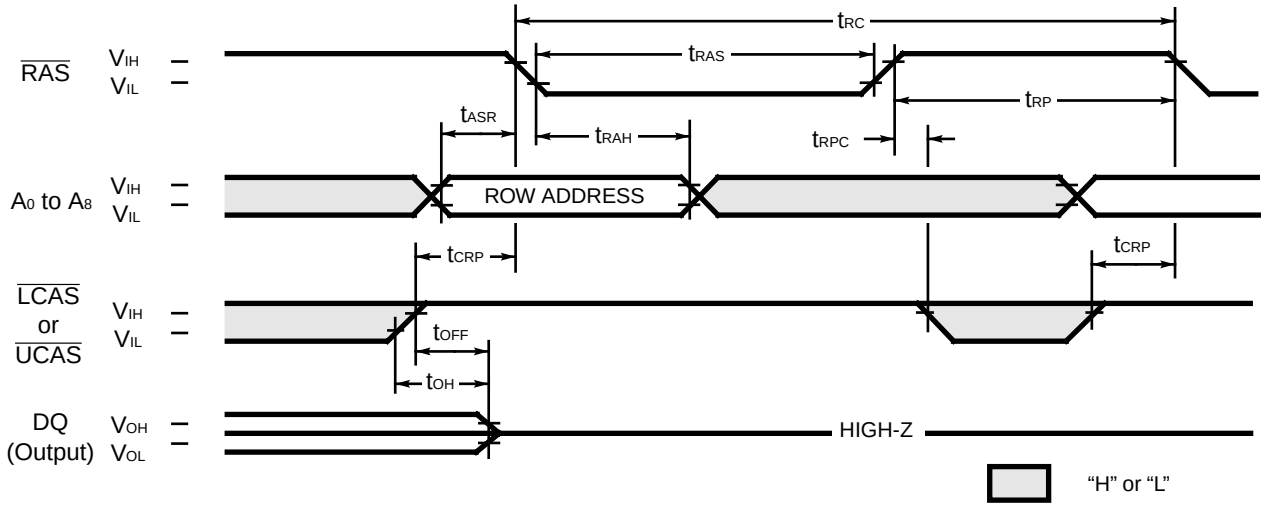
Fig. 15 – HYPER PAGE MODE READ-MODIFY-WRITE CYCLE



DESCRIPTION

During the hyper page mode of operation, the read-modify-write cycle can be executed by switching $\overline{WE}$ from High to Low after input data appears at the DQ pins during a normal cycle.

Fig. 16 – $\overline{RAS}$-ONLY REFRESH ($\overline{WE}$ = $\overline{OE}$ = "H" or "L")

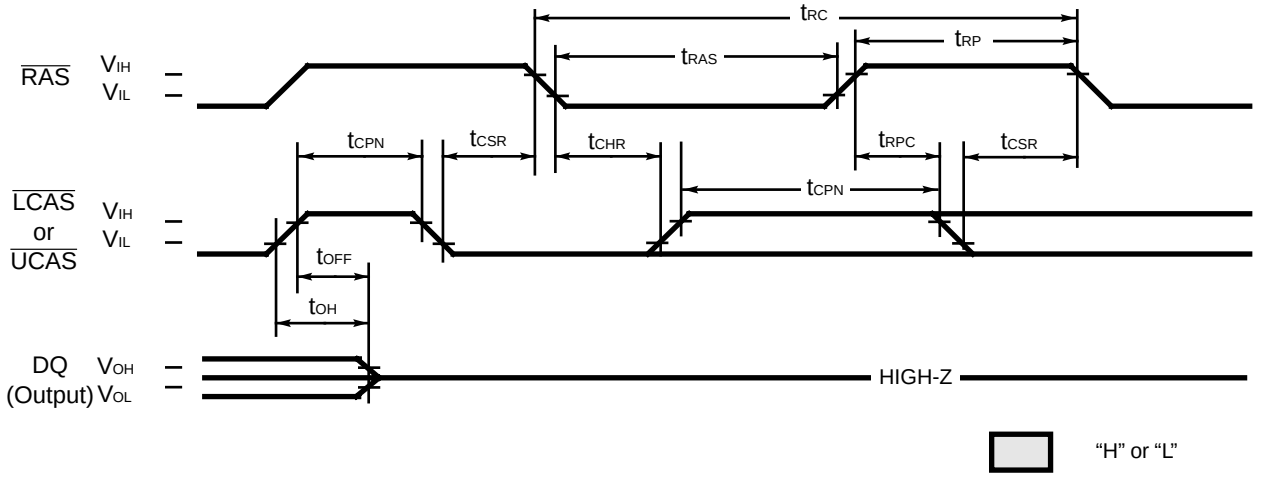


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 512 row addresses every 8.2-milliseconds. Three refresh modes are available: $\overline{RAS}$-only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$-only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{LCAS}$ and $\overline{UCAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$-only refresh, DQ pins are kept in a high-impedance state.

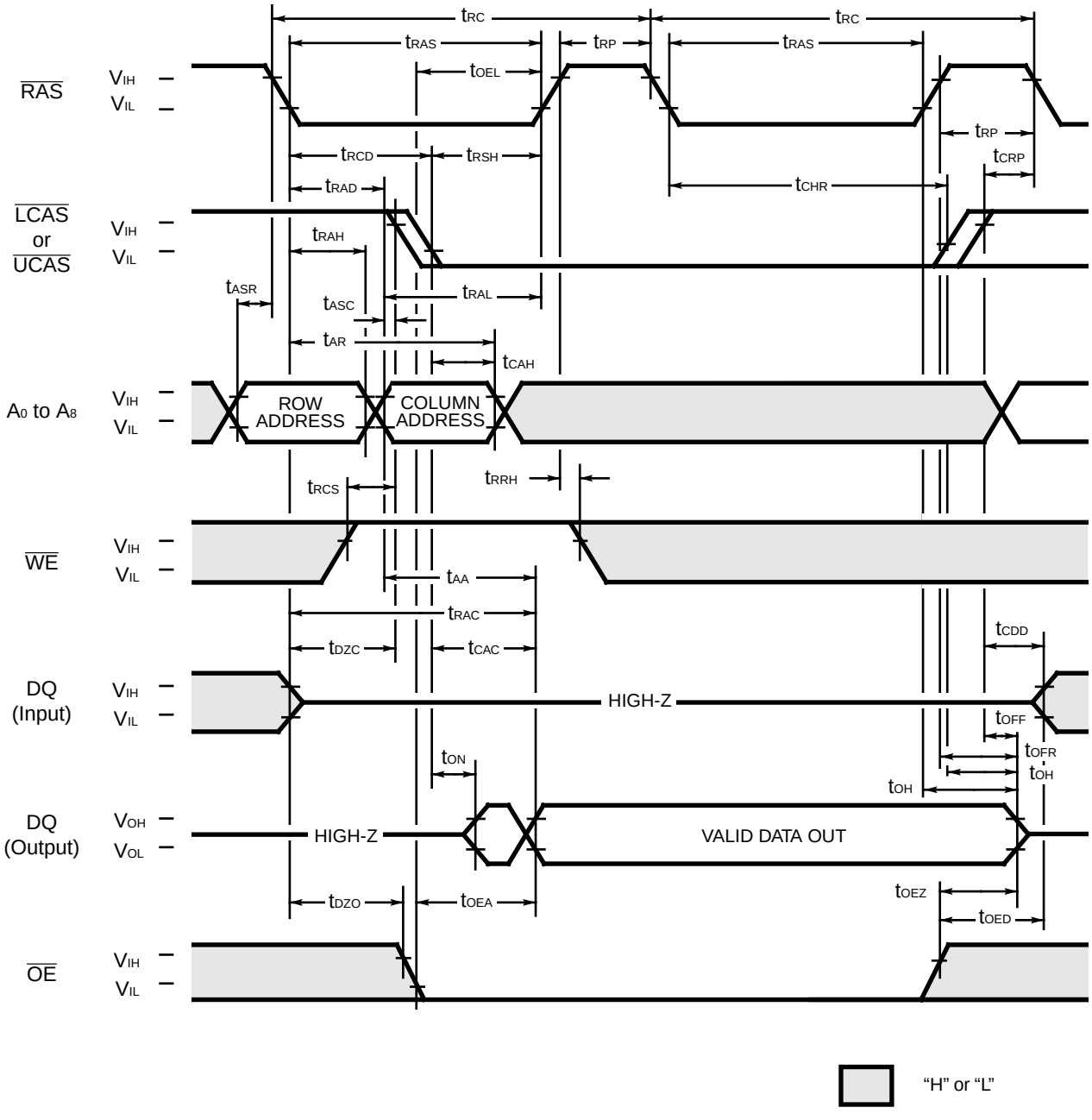
Fig. 17 – $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH (ADDRESSES = $\overline{WE}$ = $\overline{OE}$ = "H" or "L")



DESCRIPTION

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{LCAS}$ or $\overline{UCAS}$ is held Low for the specified setup time (t_{CSR}) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

Fig. 18 – HIDDEN REFRESH CYCLE

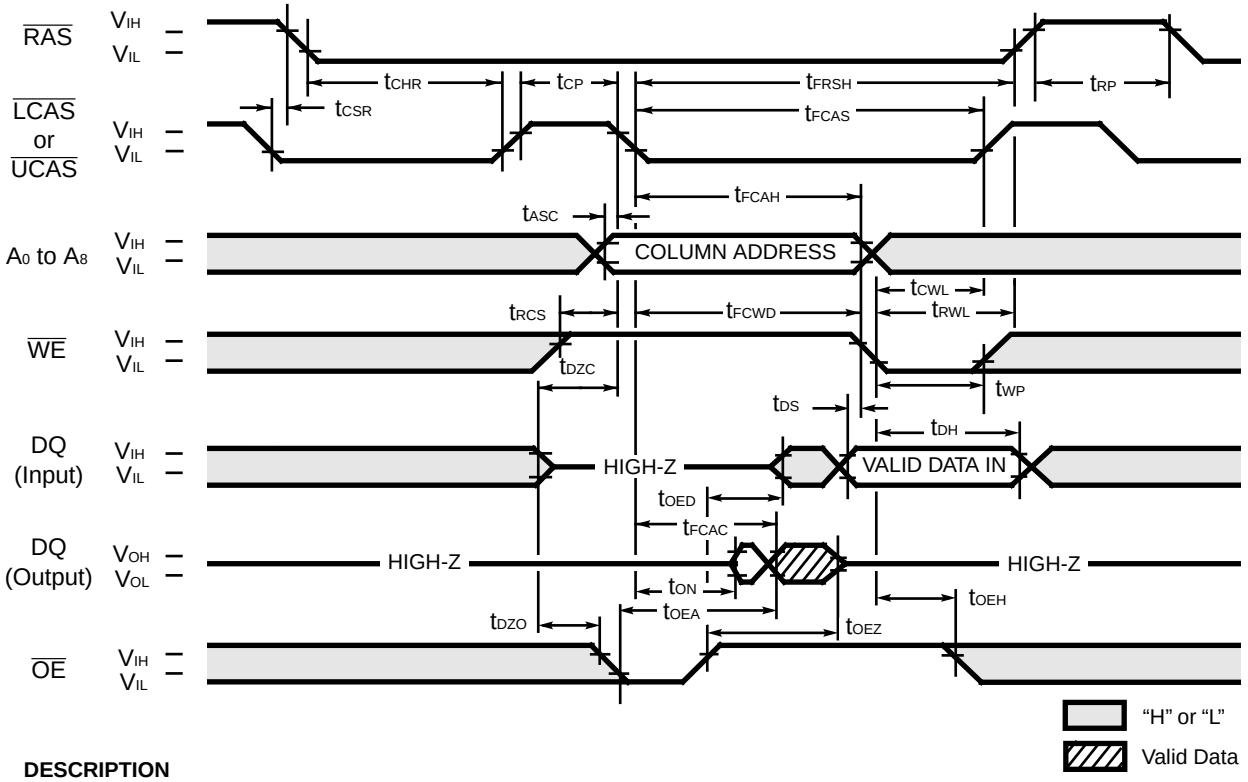


DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ and cycling $\overline{\text{RAS}}$. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh capability.

MB81V4265S-60/-70/-60L/-70L

Fig. 19 – $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DESCRIPTION

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh circuitry. After a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle, if $\overline{LCAS}$ or $\overline{UCAS}$ makes a transition from High to Low while $\overline{RAS}$ is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Address: Bits A_0 through A_8 are defined by the on-chip refresh counter.
Column Address: Bits A_0 through A_8 are defined by latching levels on A_0 to A_8 at the second falling edge of $\overline{LCAS}$ or $\overline{UCAS}$.

The $\overline{CAS}$-before-$\overline{RAS}$ Counter Test procedure is as follows;

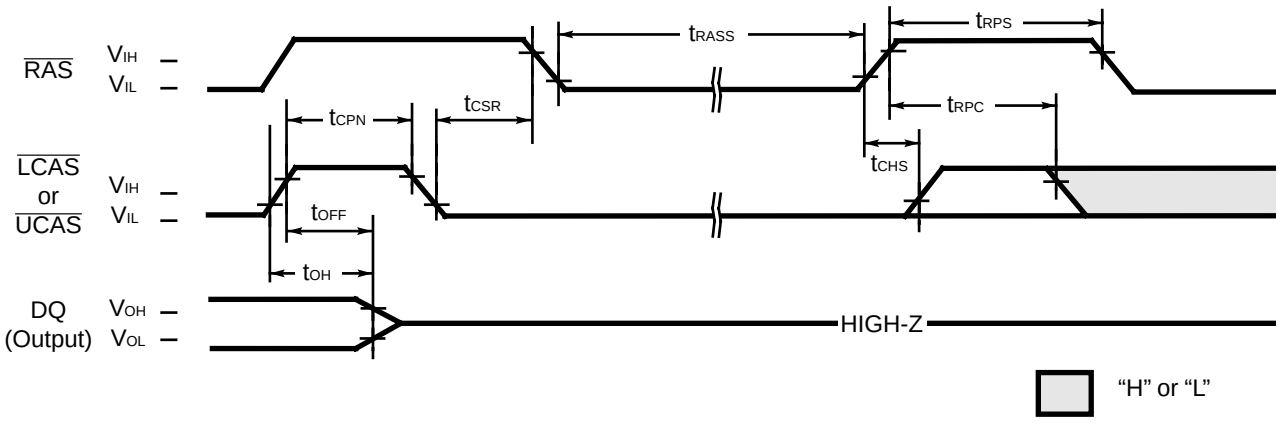
1) Normalize the internal refresh address counter by using 8 $\overline{RAS}$-only refresh cycles.
2) Use the same column address throughout the test.
3) Write "0" to all 512 row addresses at the same column address by using CBR refresh counter test cycles.
4) Read "0" written in procedure 3) by using normal read cycle and check; after reading "0" and check are completed (or simultaneously), write "1" to the same addresses by using normal write cycle (or read-modify-write cycle).
5) Read and check data "1" written in procedure 4) by using CBR refresh counter test cycle for all 512 memory locations.
6) Reverse test data and repeat procedures 3), 4), and 5).

(At recommended operating conditions unless otherwise noted.)

No.	Parameter	Symbol	MB81V4265S-60/60L		MB81V4265S-70/70L		Unit
			Min.	Max.	Min.	Max.	
90	Access Time from $\overline{CAS}$	t_{FCAC}	—	55	—	55	µs
91	Column Address Hold Time	t_{FCAH}	30	—	30	—	ns
92	$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{FCWD}	80	—	80	—	ns
93	$\overline{CAS}$ Pulse Width	t_{FCAS}	55	—	55	—	µs
94	$\overline{RAS}$ Hold Time	t_{FRSH}	55	—	55	—	ns
95	$\overline{CAS}$ Hold Time	t_{FCSH}	85	—	85	—	ns

Note: Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle only.

Fig. 20 – SELF REFRESH CYCLE (A_0 to A_8 = $\overline{WE}$ = $\overline{OE}$ = "H" or "L")



(At recommended operating conditions unless otherwise noted.)

No.	Parameter	Symbol	MB81V4265S-60/60L		MB81V4265S-70/70L		Unit
			Min.	Max.	Min.	Max.	
74	$\overline{RAS}$ Pulse Width	t_{RASS}	100	—	100	—	µs
75	$\overline{RAS}$ Precharge Time	t_{RPS}	104	—	119	—	ns
76	$\overline{CAS}$ Hold Time	t_{CHS}	–50	—	–50	—	ns

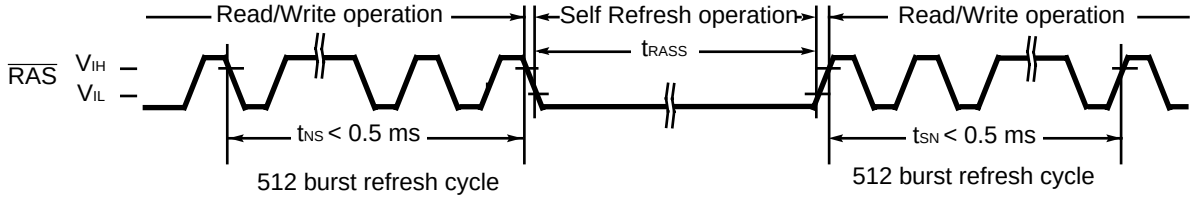
Note: Assumes Self Refresh cycle only.

DESCRIPTION

The Self Refresh cycle provides a refresh operation without external clock and external Address. Self Refresh control circuit on chip is operated in the Self Refresh cycle and refresh operation can be automatically executed using internal refresh address counter and timing generator.
If $\overline{CAS}$ goes to "L" before $\overline{RAS}$ goes to "L" (CBR) and the condition of $\overline{CAS}$ "L" and $\overline{RAS}$ "L" is kept for term of t_{RASS} (more than 100 µs), the device can enter the Self Refresh cycle. Following that, refresh operation is automatically executed at fixed intervals using internal refresh address counter during "$\overline{RAS}$=L" and "$\overline{CAS}$=L".
Exit from Self Refresh cycle is performed by toggling $\overline{RAS}$ and $\overline{CAS}$ to "H" with specified t_{CHS} min. In this time, $\overline{RAS}$ must be kept "H" with specified t_{RPS} min.
Using Self Refresh mode, data can be retained without external $\overline{CAS}$ signal during system is in standby.

Restriction for Self Refresh operation;
For Self Refresh operation, the notice below must be considered.

1) In the case that distributed CBR refresh are operated between read/write cycles
   Self Refresh cycles can be executed without special rule if 512 cycles of distributed CBR refresh are executed within t_{REF} max.
2) In the case that burst CBR refresh or distributed/burst $\overline{RAS}$-only refresh are operated between read/write cycles 512 times of burst CBR refresh or 512 times of burst $\overline{RAS}$-only refresh must be executed before and after Self Refresh cycles.

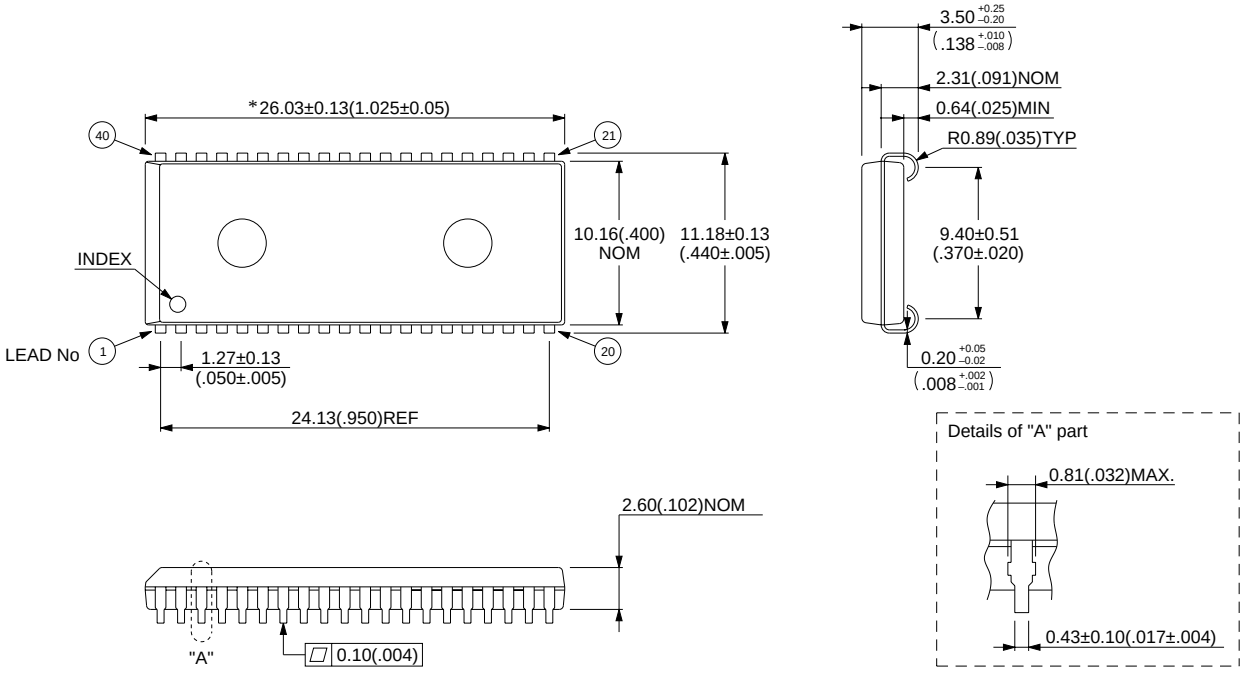


* Read/Write operation can be performed non refresh time within t_{NS} or t_{SN}.

MB81V4265S-60/-70/-60L/-70L

■ PACKAGE DIMENSIONS

40-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-40P-M01)



* Resin protrusion. (Each side: 0.15 (.006)MAX.)

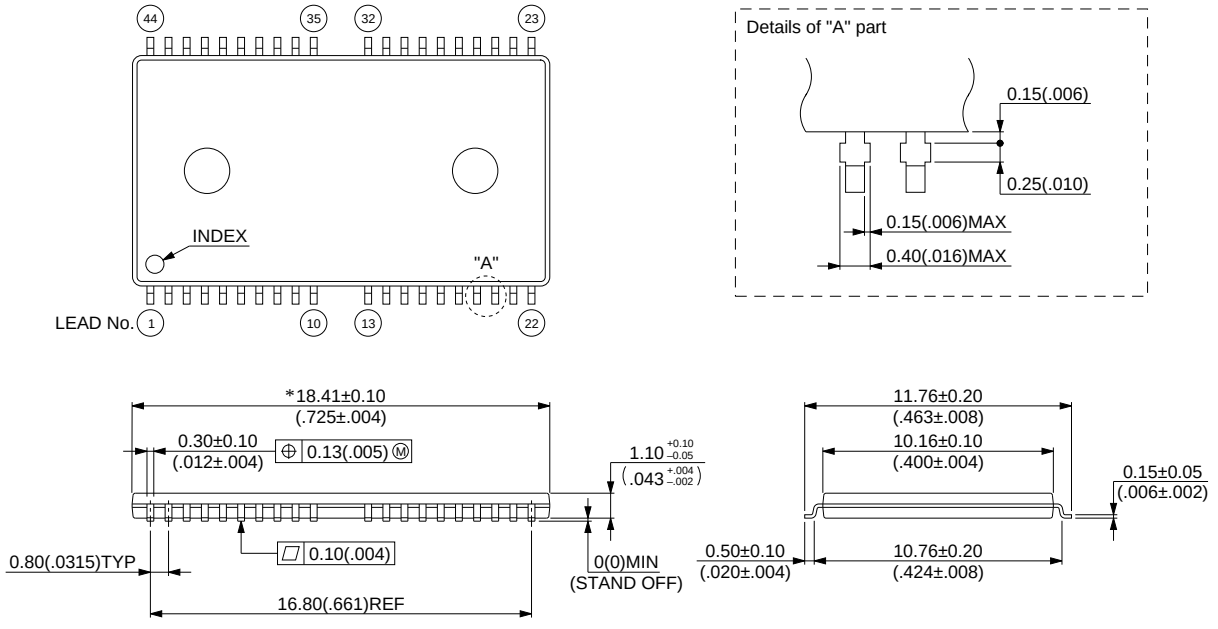
©1993 FUJITSU LIMITED C40051S-3C-1

Dimensions in mm (inches)

MB81V4265S-60/-70/-60L/-70L

■ PACKAGE DIMENSIONS

44-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-44P-M07)



* Resin protrusion. (Each side: 0.15 (.006)MAX.)

© 1994 FUJITSU LIMITED F44016S-1C-2

Dimensions in mm (inches)

MB81V4265S-60/-70/-60L/-70L

FUJITSU LIMITED

For further information please contact:

Japan
FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
KAWASAKI PLANT, 4-1-1, Kamikodanaka
Nakahara-ku, Kawasaki-shi
Kanagawa 211-88, Japan
Tel: (044) 754-3763
Fax: (044) 754-3329

North and South America
FUJITSU MICROELECTRONICS, INC.
Semiconductor Division
3545 North First Street
San Jose, CA 95134-1804, U.S.A.
Tel: (408) 922-9000
Fax: (408) 432-9044/9045

Europe
FUJITSU MIKROELEKTRONIK GmbH
Am Siebenstein 6-10
63303 Dreieich-Buchschlag
Germany
Tel: (06103) 690-0
Fax: (06103) 690-122

Asia Pacific
FUJITSU MICROELECTRONICS ASIA PTE. LIMITED
#05-08, 151 Lorong Chuan
New Tech Park
Singapore 556741
Tel: (65) 281-0770
Fax: (65) 281-0220

F9704
© FUJITSU LIMITED Printed in Japan

All Rights Reserved.

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

FUJITSU semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).
CAUTION:
Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with FUJITSU sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Control Law of Japan, the prior authorization by Japanese government should be required for export of those products from Japan.